The Invention Claimed Is

1. First-in/first-out memory circuitry comprising:

first and second Gray code counter circuitries respectively counting write and read clock signals;

Gray code subtractor circuitry subtracting counts provided by the counter circuitries; and

shift register circuitry shifting in write data words in synchronism with the write clock signal and outputting one of those data words selected based on subtraction information from the subtractor circuitry.

2. The memory circuitry defined in claim 1 further comprising:

detector circuitry configured to detect predetermined subtraction information to indicate that a predetermined capacity condition of the shift register circuitry has been reached.

3. The memory circuitry defined in claim 1 wherein the capacity condition is an empty condition.

4. The memory circuitry defined in claim 2 wherein the capacity condition is a full condition.

5. The memory circuitry defined in claim 1 wherein the first counter circuitry counts at twice the write clock rate.

6. The memory circuitry defined in claim 5 wherein the second counter circuitry counts in double increments of the Gray code.

7. The memory circuitry defined in claim 1 wherein the subtractor circuitry comprises:

second shift register circuitry shifting in count information from the first counter circuitry; and

selection circuitry selecting count information from the second shift register circuitry based on count information from the second counter.

8. The memory circuitry defined in claim 7 wherein the selection circuitry is configured to decode the count information from Gray code.

9. The memory circuitry defined in claim 1 wherein the shift register circuitry comprises:

shift register components shifting in the write data words; and

selection circuitry selecting a data word from the shift register components based on the subtraction information.

10. The memory circuitry defined in claim 9 wherein the selection circuitry is configured to decode the count information from Gray code.

11. The memory circuitry defined in claim 1 wherein the shift register circuitry comprises:

a series of alternating master and slave latch circuitries configured to transfer write data words from each master latch circuitry to a succeeding

slave latch circuitry and to alternately transfer write data words from each slave latch circuitry to a succeeding master latch circuitry during each cycle of the write clock signal.

12. The memory circuitry defined in claim 11 wherein the shift register circuitry further comprises:

selection circuitry configured to selectively output a data word from any of the master and slave latch circuitries.

13. The memory circuitry defined in claim 7 wherein the second shift register circuitry comprises:

a series of alternating master and slave latch circuitries configured to transfer count information from each master latch circuitry to a succeeding slave latch circuitry and to alternately transfer count information from each slave latch circuitry to a succeeding master latch circuitry during each cycle of the write clock signal.

14. The memory circuitry defined in claim 13 wherein the selection circuitry is configured to select count information from any of the slave latch circuitries.

15. A programmable logic device including memory circuitry as defined in claim 1.

16. A data processing system comprising:

processor circuitry; and

memory circuitry as defined in claim 1 coupled to the processor circuitry.

17. A printed circuit board on which is mounted memory circuitry as defined in claim 1.

18. The printed circuitry board defined in claim 17 on which is further mounted processor circuitry coupled to the memory circuitry.

19. First-in/first-out memory circuitry comprising:

write counter circuitry configured to count, in a Gray code, half cycles of a write clock signal that is synchronized with successive write data words;

read counter circuitry configured to count, in double increments of the Gray code, a read clock signal;

first shift register circuitry configured to shift in Gray code count data produced by the write counter and to output a Gray code count selected based on double-increment count data produced by the read counter circuitry; and

20. The memory circuitry defined in claim 19 further comprising:

detector circuitry configured to compare the Gray code count output by the first shift register circuitry to a predetermined count indicative of a particular capacity condition of the second shift register circuitry.

21. The memory circuitry defined in claim 20 wherein the capacity condition is an empty condition.

22. The memory circuitry defined in claim 20 wherein the capacity condition is an empty condition.

23. The memory circuitry defined in claim 19 wherein the first shift register circuitry comprises:

shift register components shifting in the Gray code count data; and

selection circuitry selecting Gray code count data in the shift register components based on Gray code decoding of the double-increment count data.

24. The memory circuitry defined in claim 23 wherein the shift register components comprise:

a series of alternating master and slave latch circuitries configured to transfer Gray code count data from each master latch circuitry to a succeeding slave latch circuitry and to alternately transfer Gray code count data from each slave latch circuitry to a succeeding master latch circuitry during each cycle of the write clock signal.

25. The memory circuitry defined in claim 24 wherein the selection circuitry is configured to select Gray code count data in any of the slave latch circuitries.

26. The memory circuitry defined in claim 19 wherein the second shift register circuitry comprises.

shift register components shifting in the write data words; and

selection circuitry selecting a write data word in the shift register components based on Gray code decoding of the Gray code count output by the first shift register circuitry.

27. The memory circuitry defined in claim 26 wherein the shift register components comprise:

a series of alternating master and slave latch circuitries configured to transfer write data words from each master latch circuitry to a succeeding slave latch circuitry and to alternately transfer write data words from each slave latch circuitry to a succeeding master latch circuitry during each cycle of the write clock signal.

28. The memory circuitry defined in claim 27 wherein the selection circuitry is configured to select a write data word in any of the master and slave latch circuitries.

29. Gray code subtractor circuitry comprising:

shift register circuitry receiving and shifting in a first data signal sequence based on a Gray code; and

decoder circuitry receiving a second data signal sequence based on a Gray code and selecting for output a first data signal in the shift register circuitry based on the second data signal.

30. The circuitry defined in claim 29 further comprising:

first circuitry configured to produce the first data signal sequence.

31. The circuitry defined in claim 30 further comprising:

second circuitry configured to produce the second data signal sequence.

32. The circuitry defined in claim 31 wherein the first circuitry is configured to produce the first data signal sequence in synchronism with a first clock signal, and wherein the second circuitry is configured to produce the second data signal sequence in synchronism with a second clock signal.

33. The circuitry defined in claim 32 wherein the first circuitry is configured to produce successive Gray code data signals in response to each successive half-cycle of the first clock signal.

34. The circuitry defined in claim 33 wherein the second circuitry is configured to produce successive double-increment Gray code data signals in response to each successive cycle of the second clock signal.

35. The circuitry defined in claim 29 further comprising:

first circuitry configured to produce signals having a Gray code sequence as the first data signal sequence; and

second circuitry configured to produce signals having a double-increment Gray code sequence as the second data signal sequence.